**ECE 3663**

**Design Review 1 - Schematics**

**Group: ADD**

**3/13/2012**

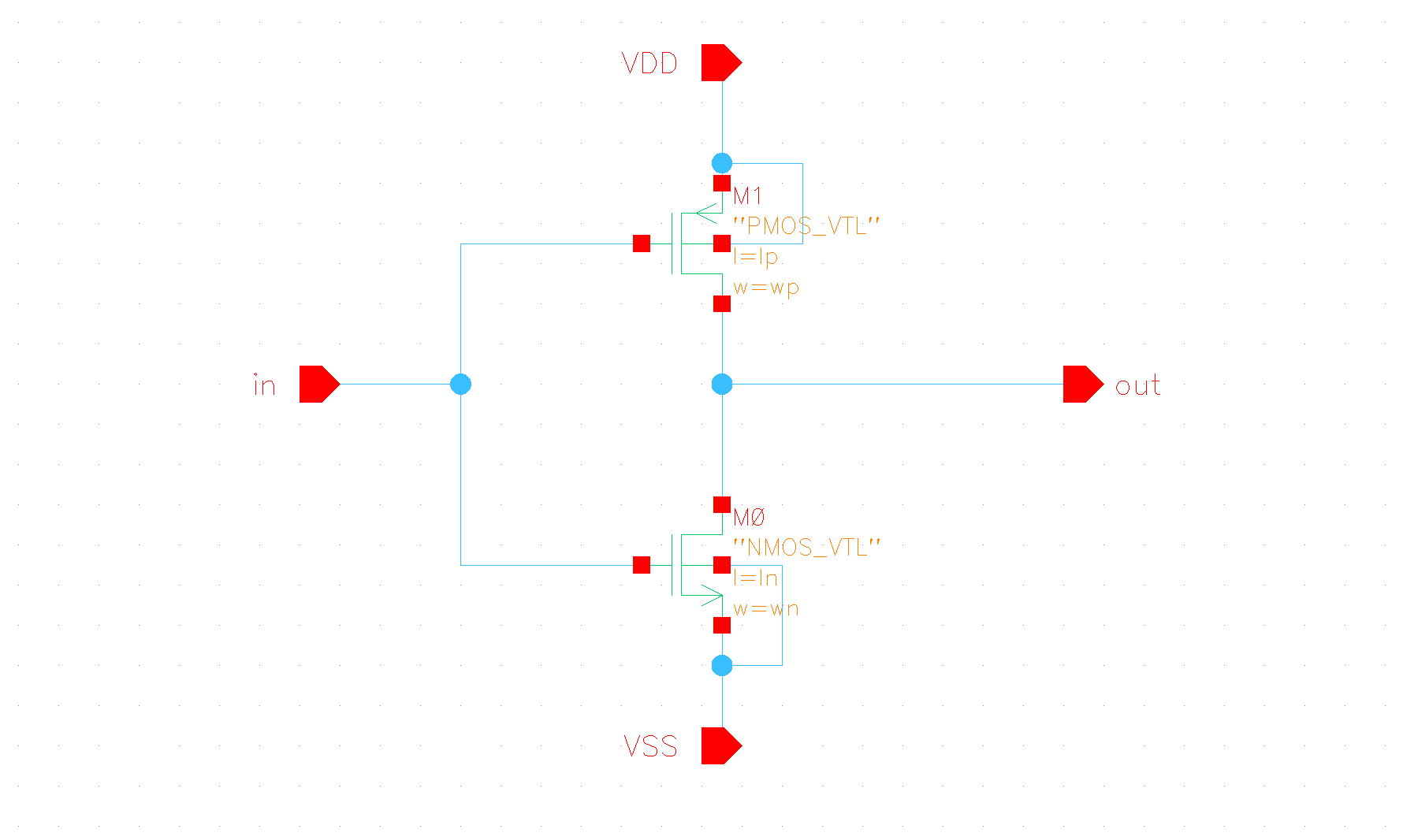
Ian Dansey (imd4hf)

Chuhong Duan (cd8dz)

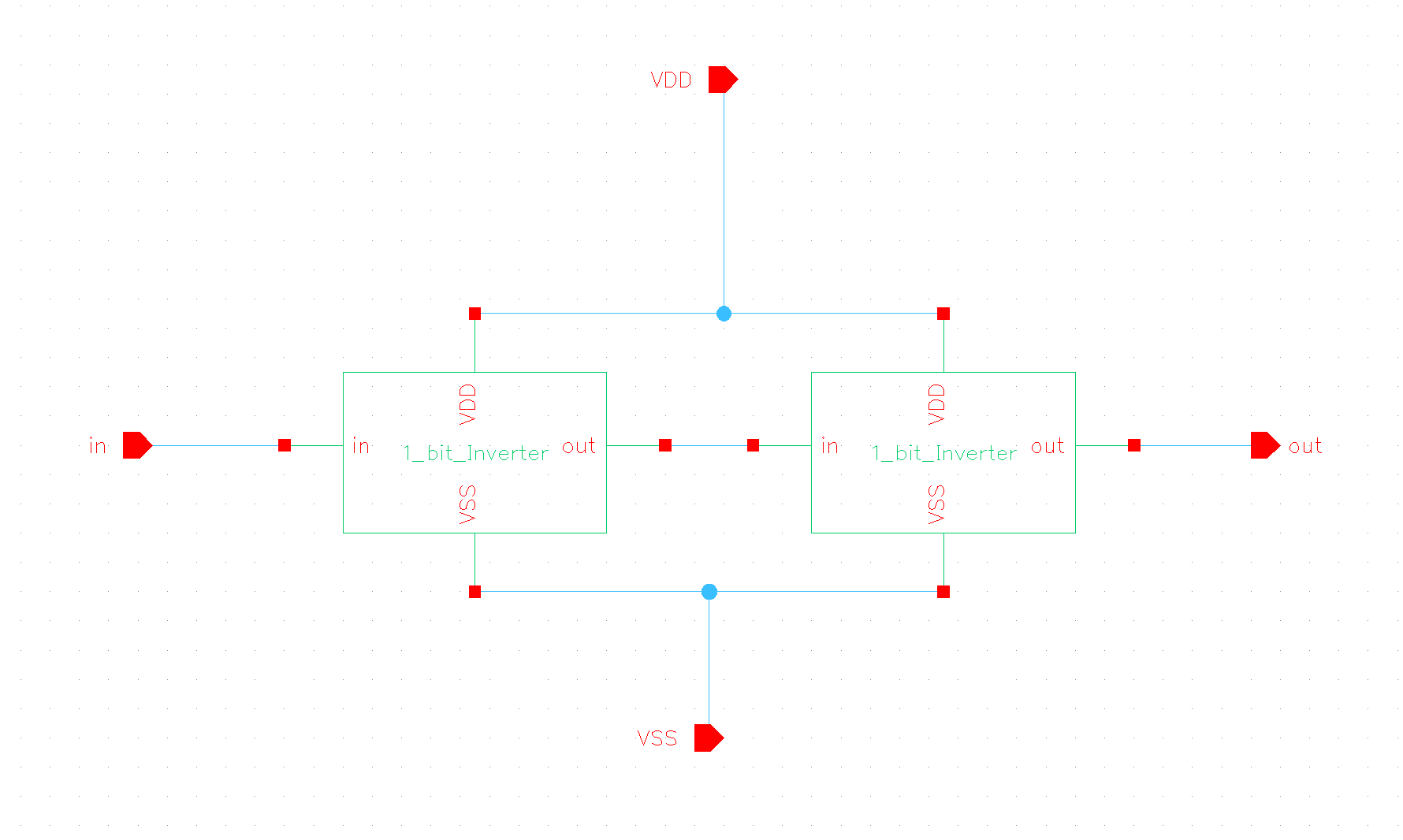
Michael Kremer (mbk2ks)

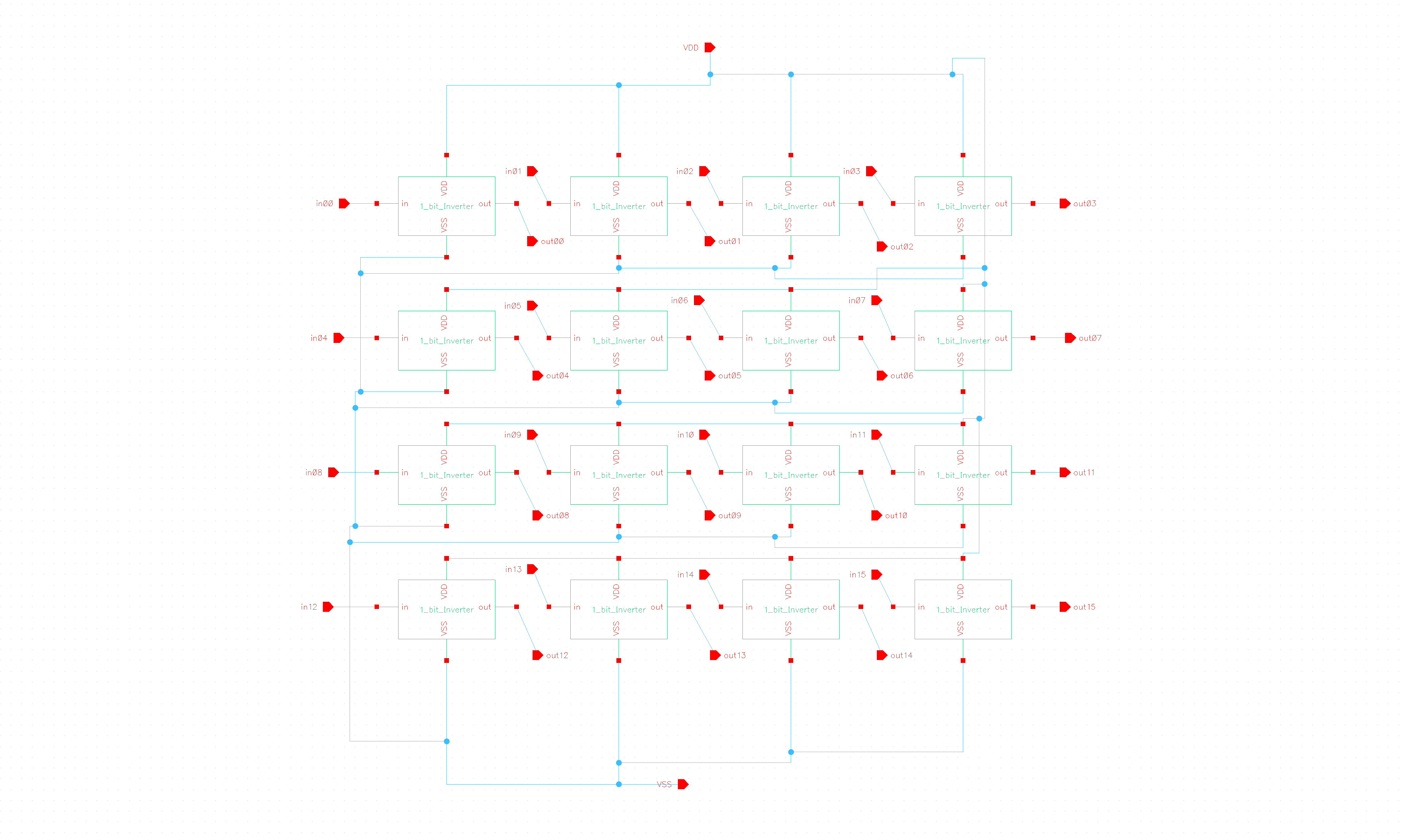
Lingtian Wan (lw9pg)

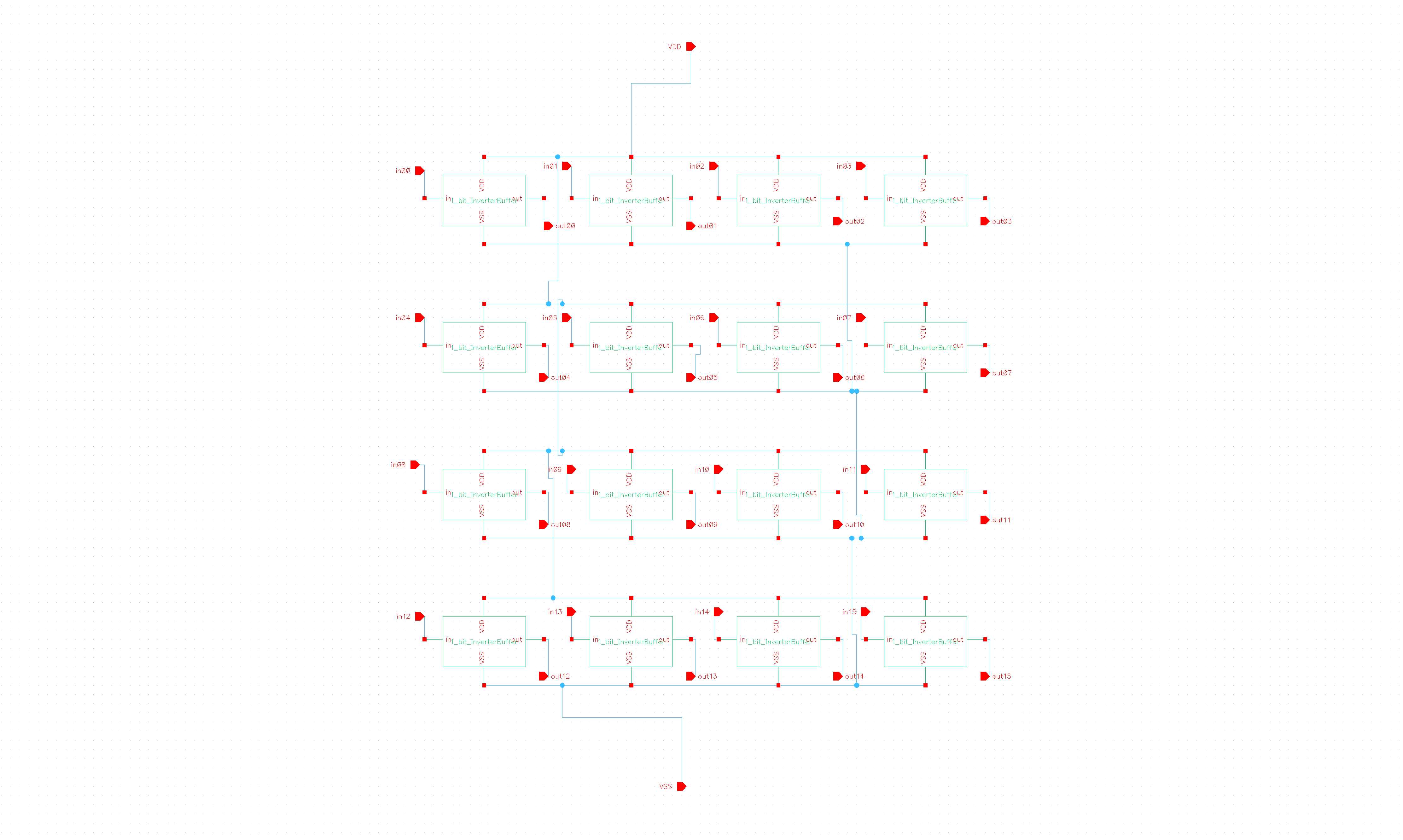
1. Basic elements required to build AND, OR, PASS and 8-1 MUX
   1. 1-bit Inverter



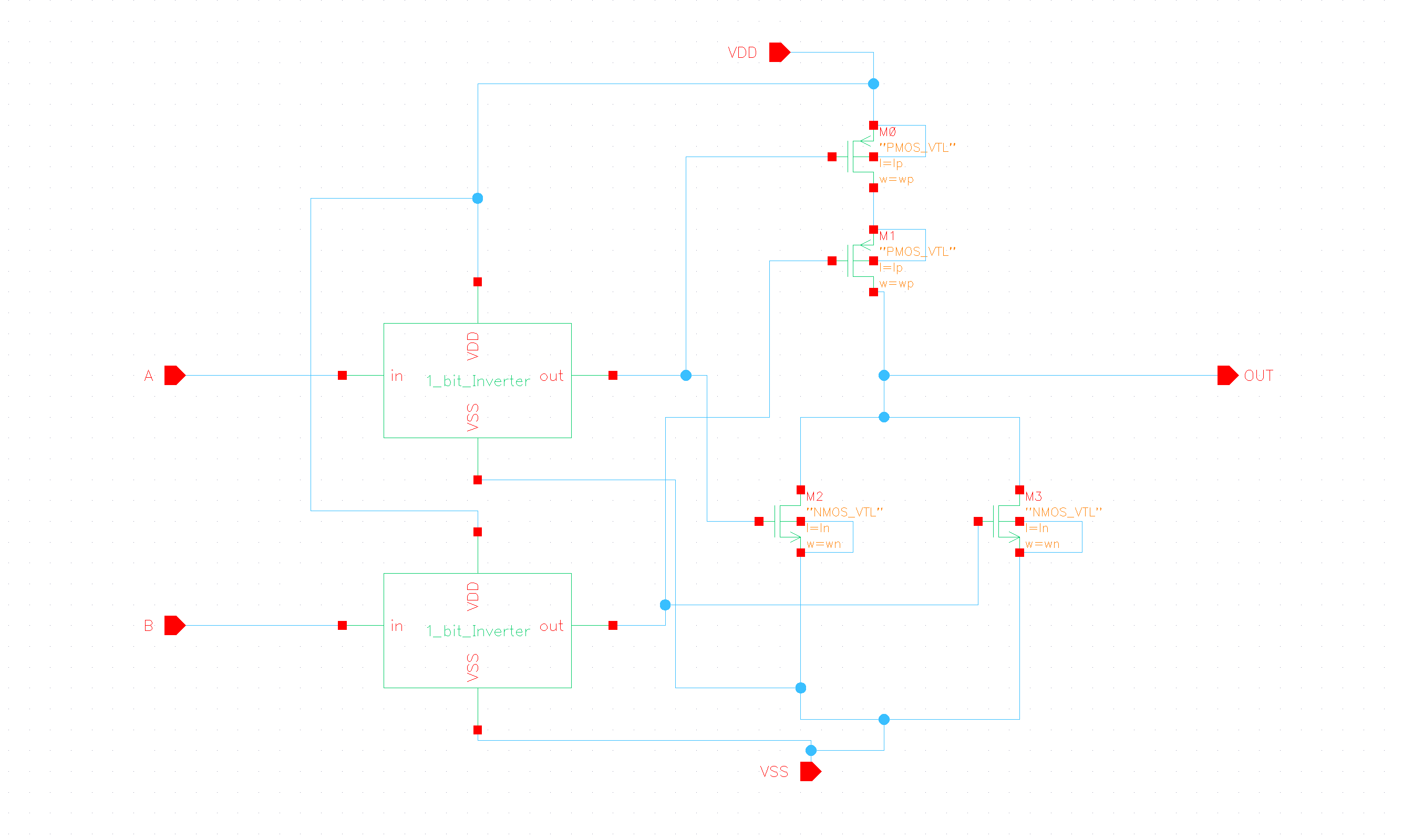
* 1. 1-bit Inverter Buffer



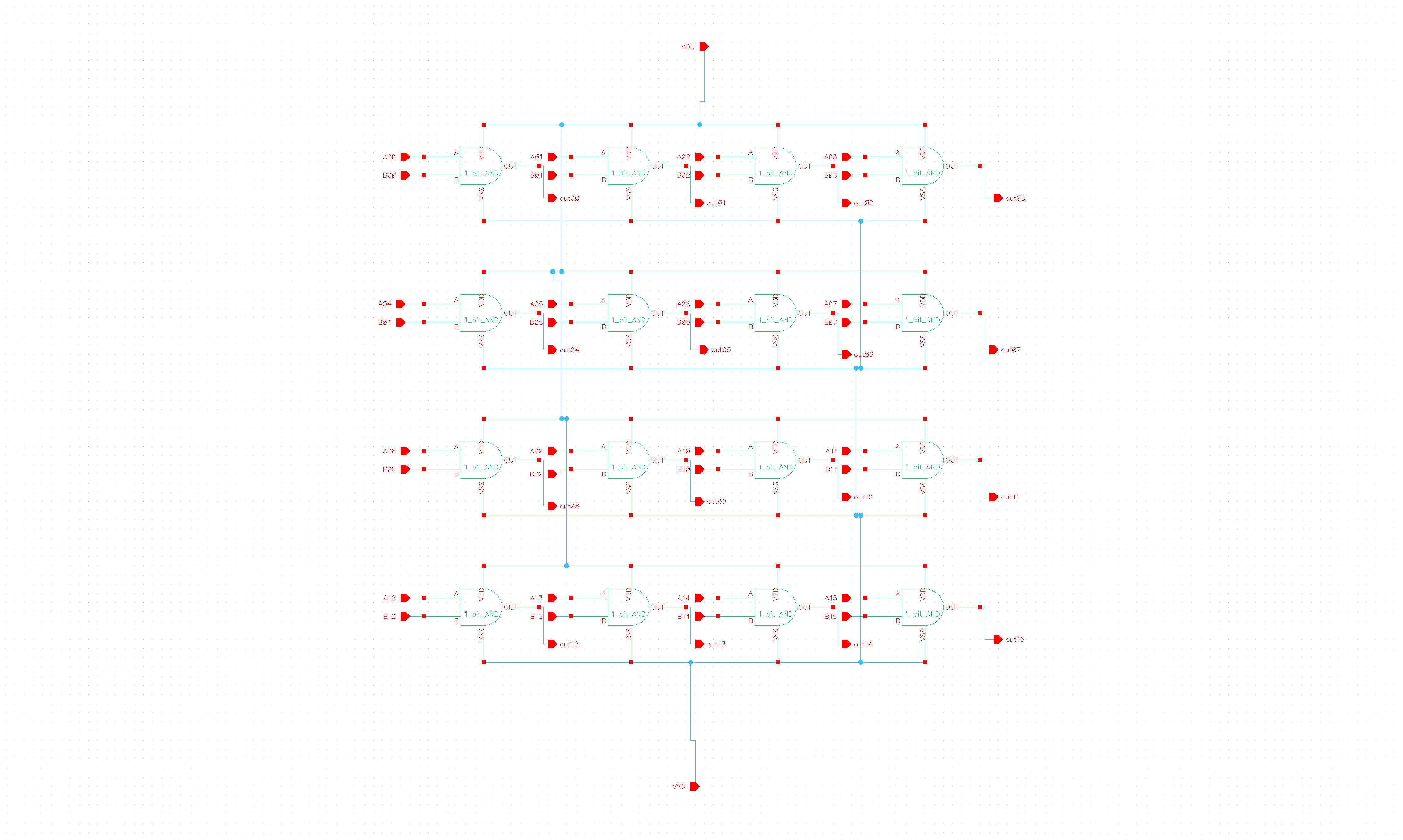
* 1. 16-bit Inverter
  2. 16-bit Inverter Buffer



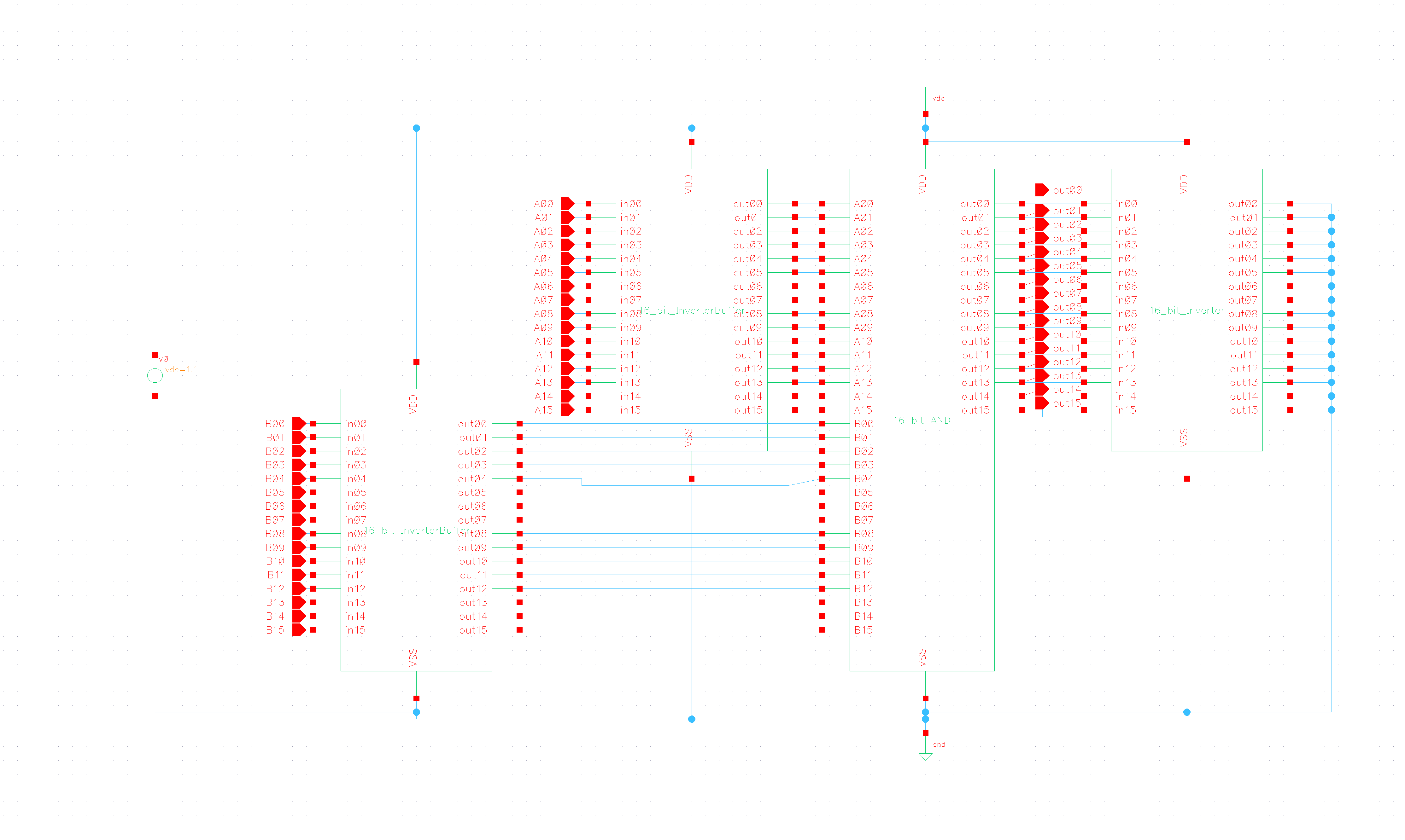
1. Schematics for AND
   1. 1-bit AND



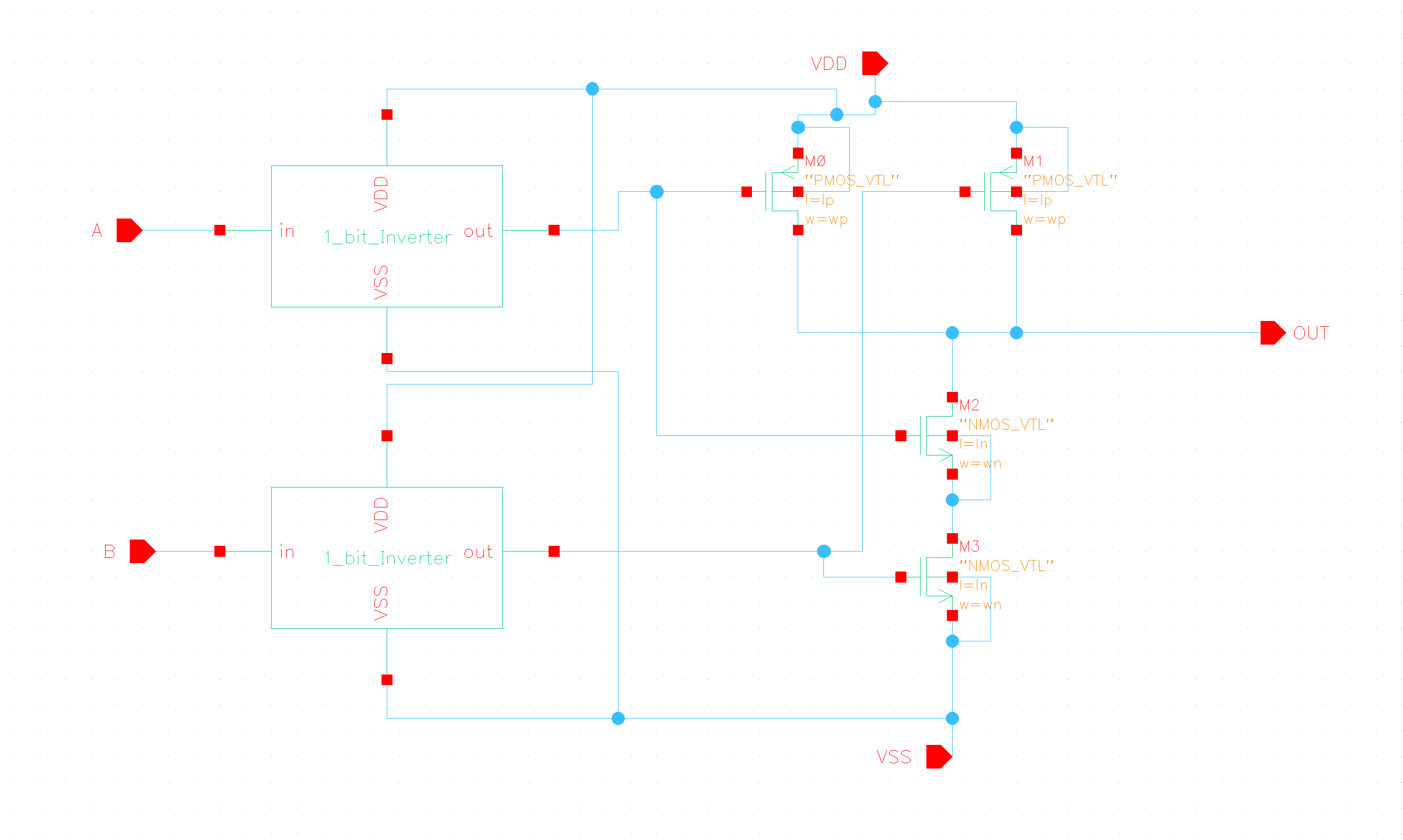
* 1. 16-bit AND



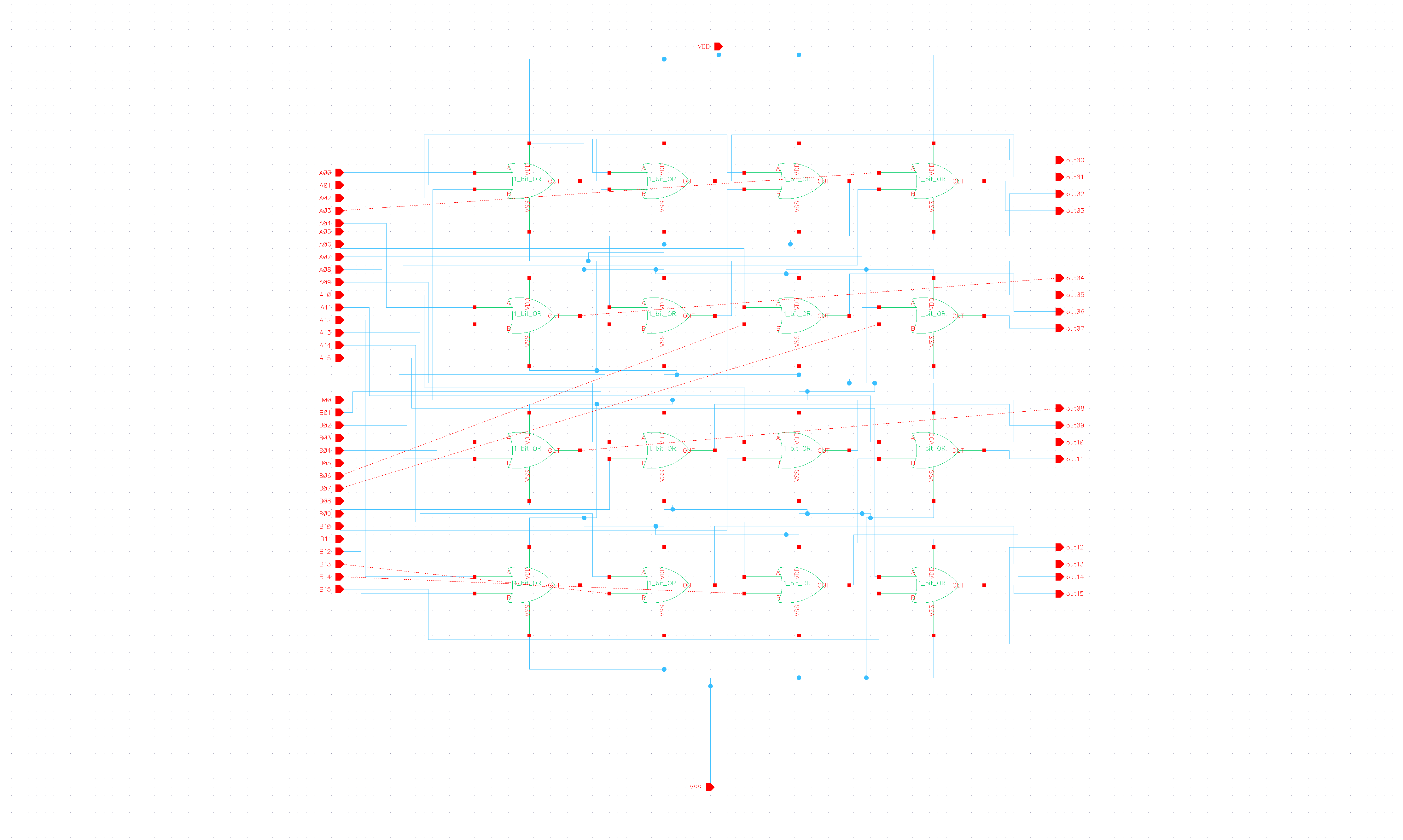
* 1. Simulation schematic of 16-bit AND



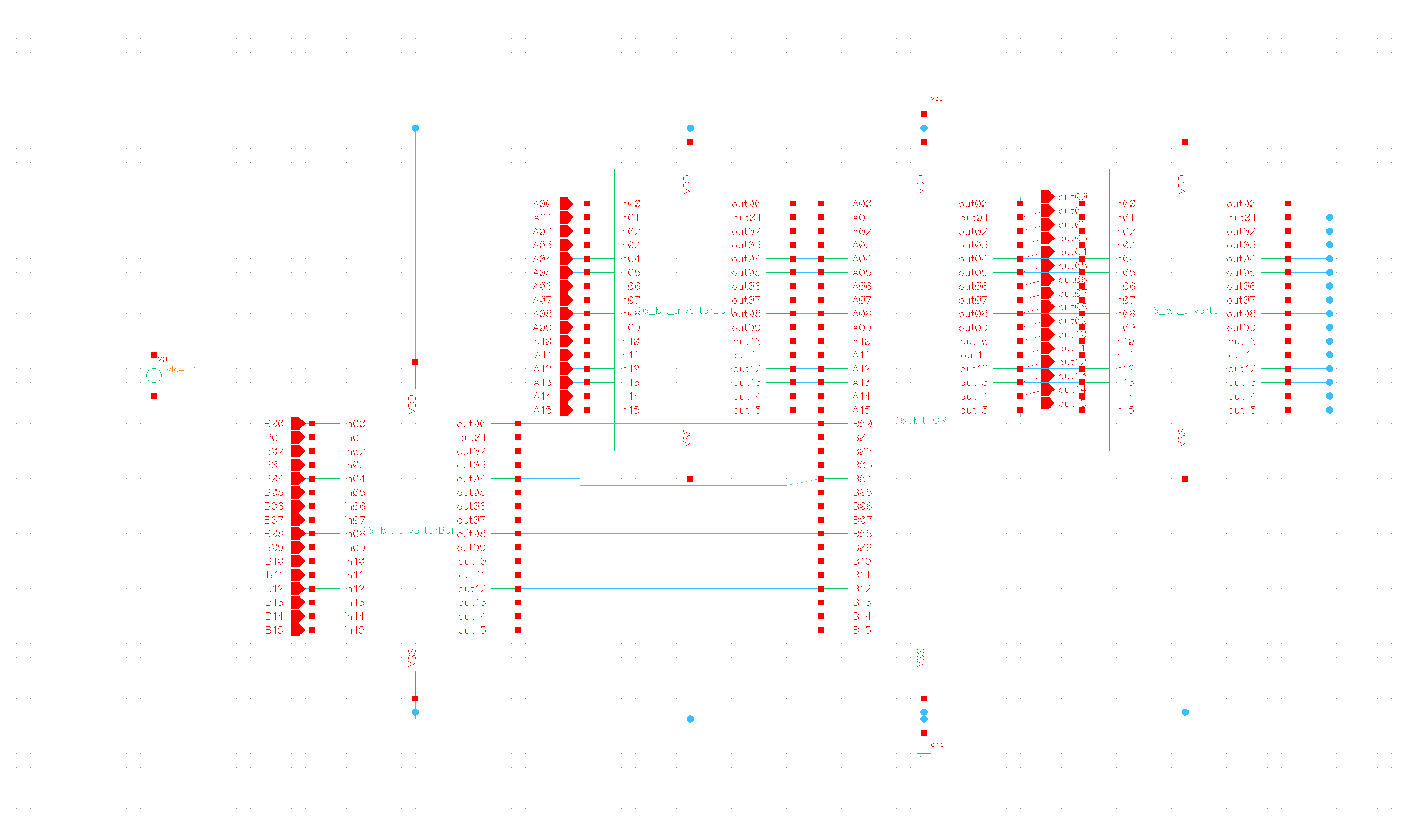
1. Schematics for OR
   1. 1-bit OR



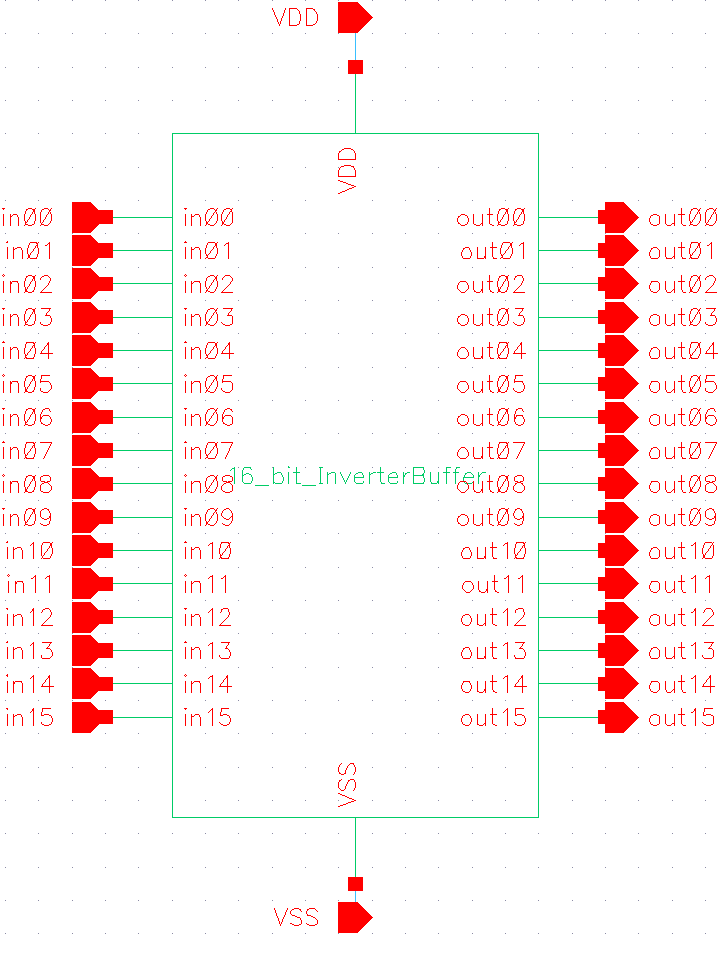
* 1. 16-bit OR



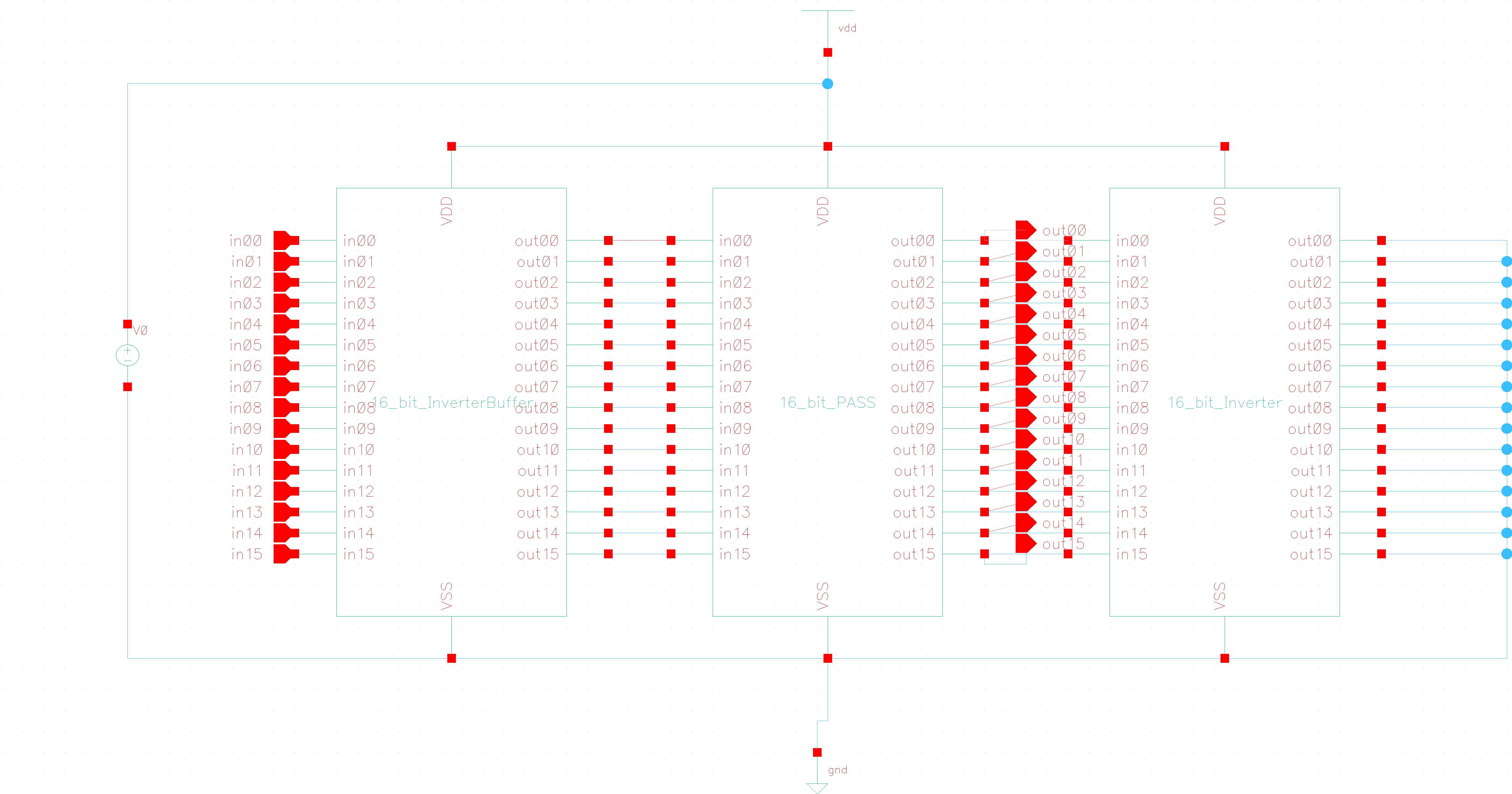
* 1. Simulation schematics for 16-bit OR



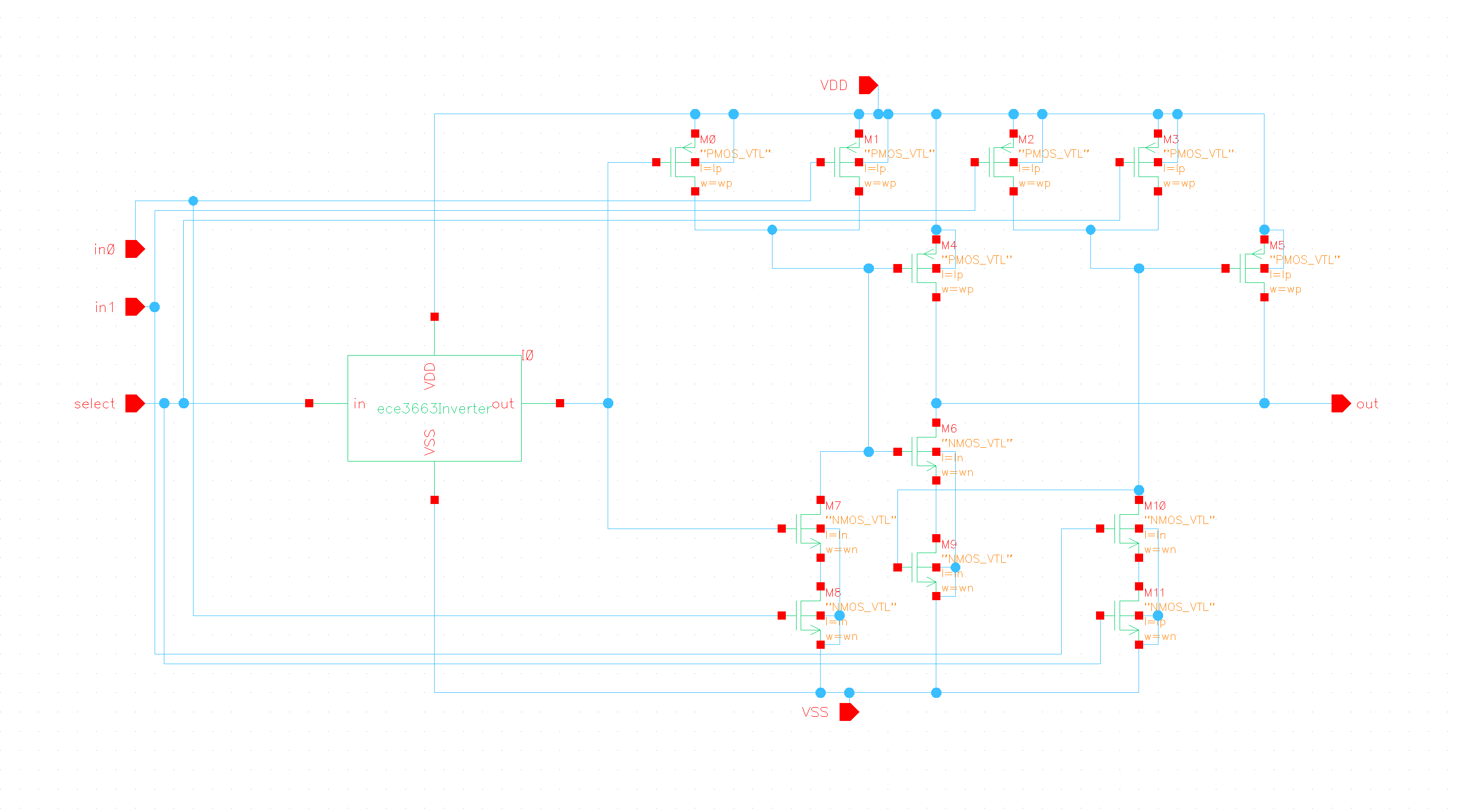
1. Schematics for PASS
   1. 16-bit PASS



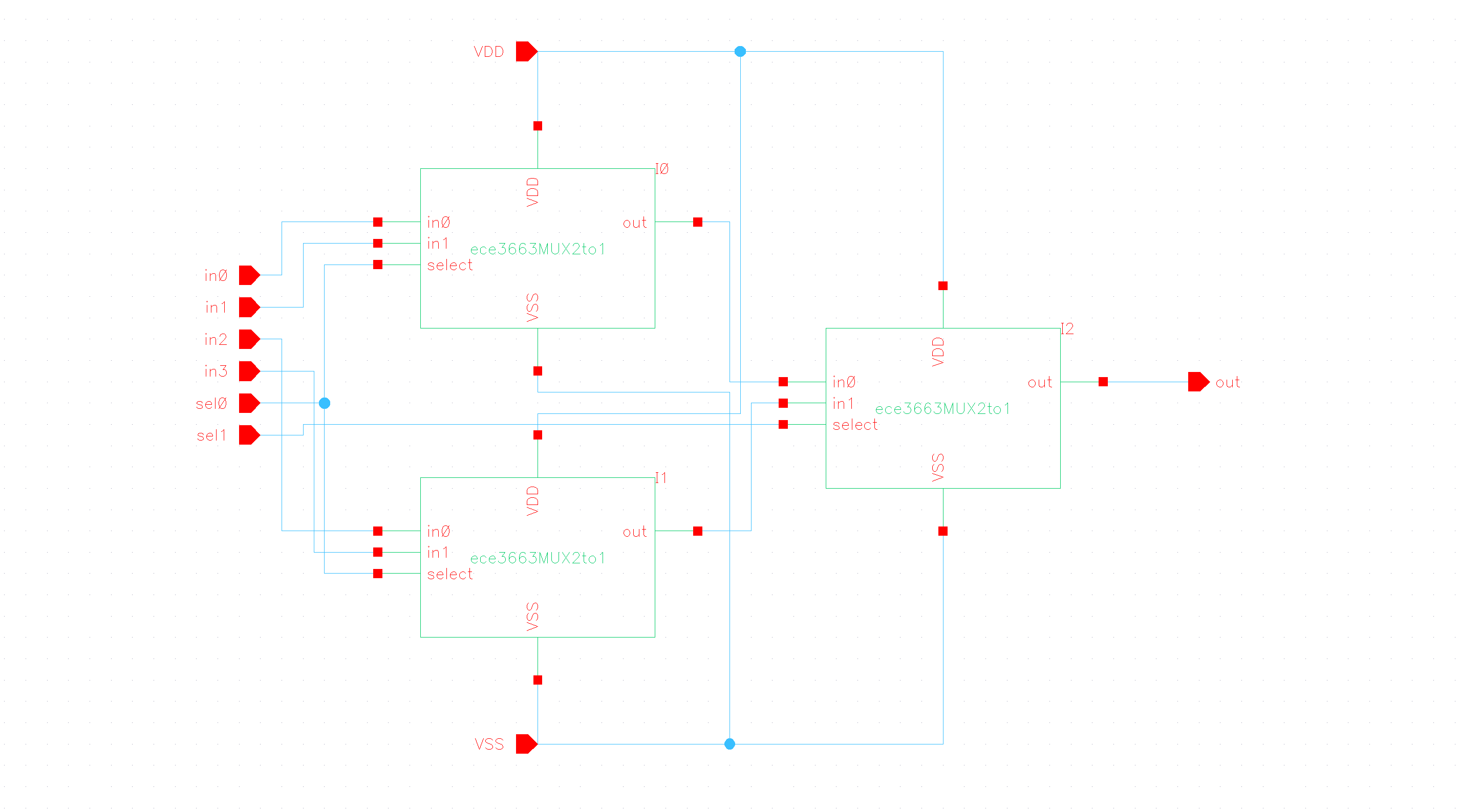
* 1. Simulation schematic for PASS:



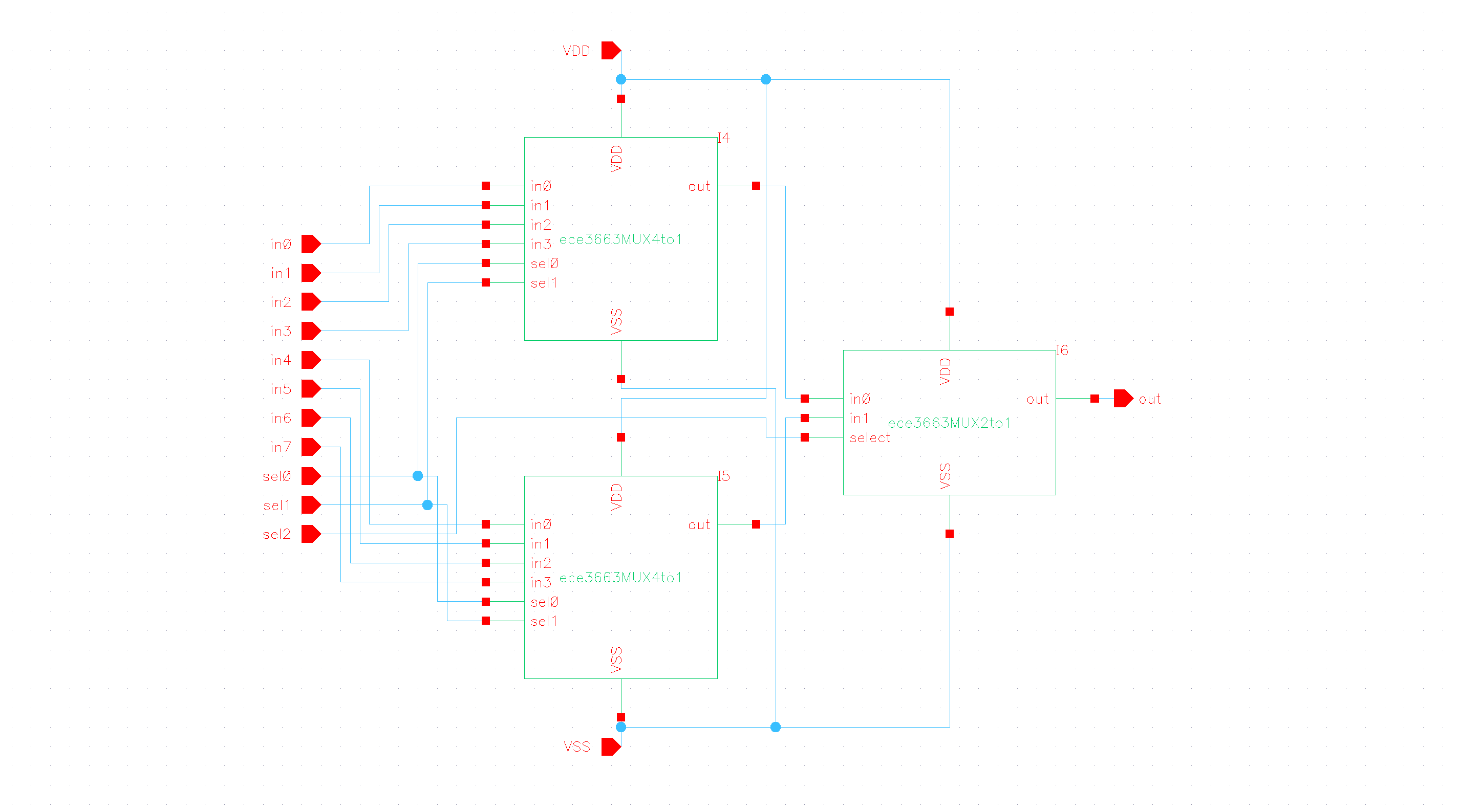
1. Schematics for 8 to 1 MUX
   1. 2:1 MUX



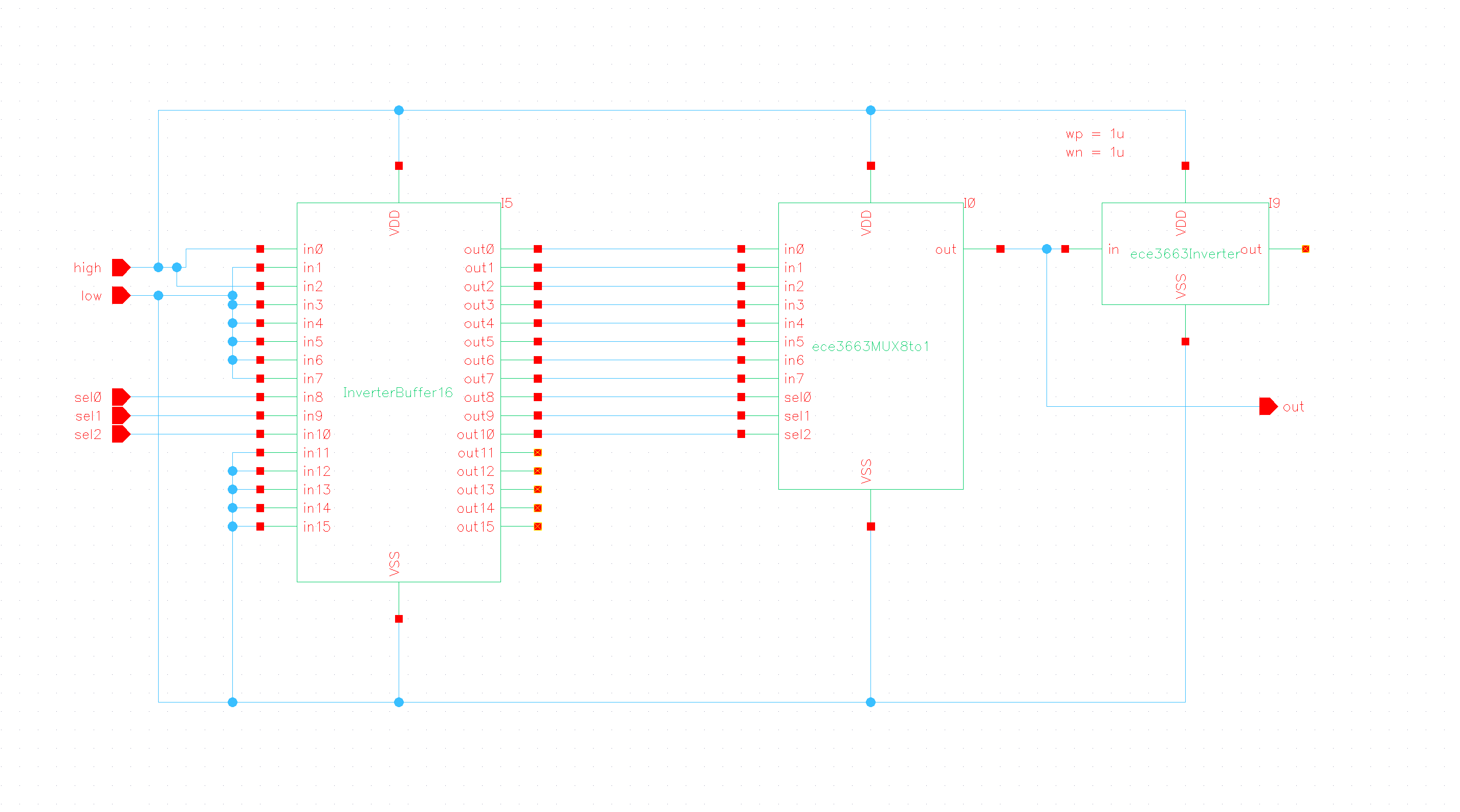
* 1. 4:1 MUX



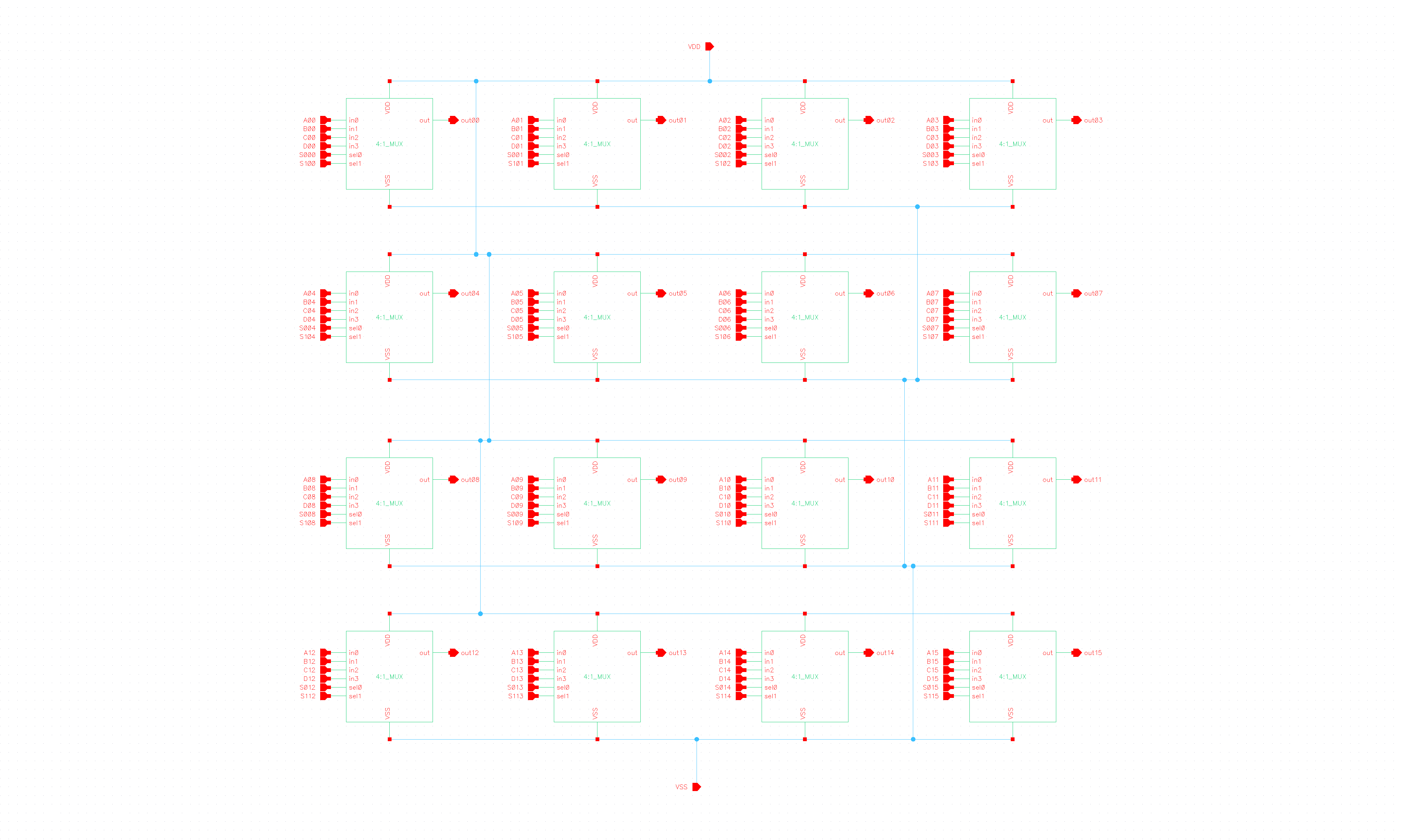
* 1. 8:1 MUX



* 1. Simulation schematic for 8:1 MUX



1. Schematic for bonus:
   1. 16-bit 4:1 MUX



* 1. Simulation schematic for bonus:

